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A Novel Low Power Full Adder Cell

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Abstract:The digital systems efficiency depends on the performance of the internal components. Hence those internal components have to be designed in such a way they provide the high speed logic with low power consumption. Full Adder is one of those kinds of component which plays an important role in the design of the systems. It is one of the primary components in most of the processors also. In this paper we have proposed a Full-Adder which uses the newer architecture. The main idea is to design the CMOS based low power Full-Adder which accounts lesser area and transistor counts. The design has been carried out using the Tanner tool V13.1.

Keywords: ***Full-Adder, Low Power, System efficiency***

I. INTRODUCTION

In the field of VLSI, Full-Adder is one of the important building blocks of the entire system. Since the invention of the Full-Adder several attempts have been made to resize its structure and use different logic implementations to produce a low power and high performance circuit. The system level advantage of the improvement in Full-Adder is the increase in the device counts on the system and resulting in the decrease in the area of the system designs.

In today's world, the trend of using the portable devices has been increased to the larger extent. In Portable devices like cellular devices, Laptops & hand held devices, the power requirement is the major issue and then comes the small area & high speed operation. Due to these complications many organizations have focussed their research on the low power VLSI field [1].

Mux based Full-Adder has been designed using Pass transistors in [1]. In [2] author has designed the Vedic Multiplier using the Full-Adders and whereas the Full-Adder has been designed using the mixed styles of pass transistors and the transmission gates. A framework for designing a low power multiplier is designed using a energy efficient Full-Adder in [3]. Brinda has designed a transmission gate Full-Adder circuit using 10Ts [4]. In this paper we have come with the new architecture for Full-Adder. Here we have used the multiplexers and Xor circuits to design the Full-Adder circuits. The rest of the paper is organised as follows. Section II describes the Full-Adder architectures. Results and Observations are discussed in the Section III. Finally Conclusion and References are provided in the Sections IV and Sections V respectively.

II. FULL-ADDER ANALYSIS

A basic Full Adder consists of three inputs and two outputs. The Basic expression used to implement the Full-Adder circuit is given in equations 1 and 2.

$$Sum = A \oplus B \oplus C \quad \text{..... (1)}$$
$$Carry = AB + BC + CA \quad \text{..... (2)}$$

The Existing architecture of the Full-Adder design is shown in the figure 1. The existing architecture consists of the XOR and Multiplexers circuits. In this circuit the XORs are used in the Cascade format to generate the Sum of the Full-Adder and then the partial output of the Sum of Full-Adder has been used to design the carry out of the Full-Adder. The proposed architecture is as shown in the figure 2. In this architecture we have avoided the effect of stacking which results in low power consumption. The parallelism is also considered in the architecture. From the above discussions the proposed design will reduce the power consumption and improve the performance when compared against the existing architecture.

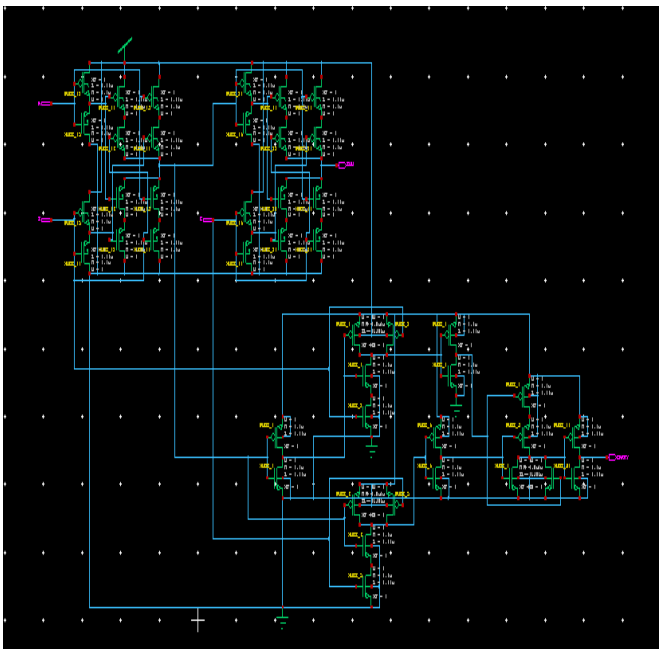

Figure 1: Existing Architecture of the Full-Adder

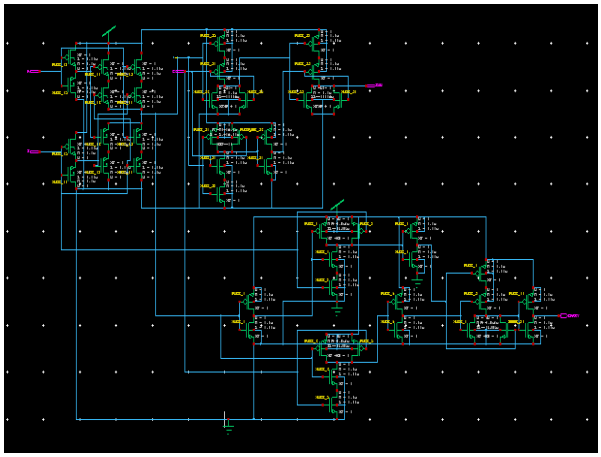

Figure 2: Proposed Architecture of the Full-Adder

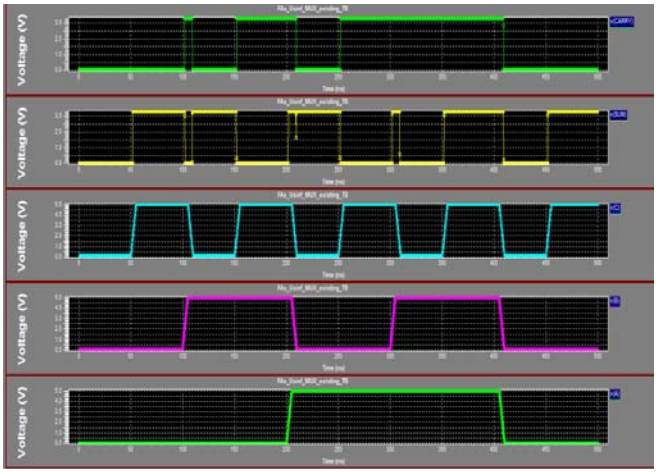

Figure 3: Result Waveforms of the Full-Adder

III. ANALYSIS OF RESULTS

The resultant waveforms of the Full-Adder are shown in the figure 3. Both the Existing and the proposed designs have been designed and simulated using the Tanner tool. The designs are analyzed as per the ASIC design methodologies. From the Table I we can observe that the proposed design has the better results compared to its counter-part existing architecture. The proposed design has gained about 19% of power against the existing design without affecting the performance of the design. The advantage of such a kind of architecture is that it can be extended to any width. Since it's an architectural creativity the design can be targeted to any technology model and gain the same amount of improvement or even more without affecting the design's quality metrics.

TABLE I: Comparison of existing and proposed Full-Adder designs

Description	Existing	Proposed	% gain
Area (Transistor counts)	**44 T**	**46 T**	**-4.5**
Timing (A to Sum)	**228.48 ns**	**228.55 ns**	**-**
Power (Avg Power)	**585.32 nW**	**473.21 nW**	**19.15**

Note :
ns = nano seconds,
T = No. Of transistors,
nW = nano watt

IV. CONCLUSION

The architectures are designed in Tanner tool with respect to ASIC design methodology. The designs are tested under typical conditions and targeted to TSMC 180nm technology kit. A typical 3.3V power supply was provided and a standard 1pF load was applied at the output of the designs. The designs were verified for all the input test vectors. The results from the table tell that the proposed design has yielded better improvement in the power compared to the existing design. Further improvement in the performance can also be done by using the faster architecture but with little trade-off in the power consumption of the device. Since the innovation of the proposed design is in the architecture, the design can be used in any larger system and can be extended to any width.

V. REFERENCES

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